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Architecture, Jun. 17-19, 1985, Boston Mass., pp. 136-144, "MU6V: A Parallel
Vector Processing System", by R. N. Ibbett, et al.

ART-UNIT: 232

PRIMARY-EXAMINER: Zache; Raulfe B.

ATTY-AGENT-FIRM: Fay, Sharpe, Beall, Fagan, Minnich & McKee

ABSTRACT:
A computer comprising a circuit for writing a group of ordered data elements
onto the main storage; a circuit for reading said group of data from the main
storage; and a circuit which is connected to the writing circuit and to the
reading circuit, and which ensures the sequence of main storage references
between said writing circuit and said reading circuit such that said reading
circuit will not read the data elements that have not yet been written by said
writing circuit among said group of data elements.

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DOCUMENT-IDENTIFIER: US 4985827 A

TITLE: Computer for synchronized read and write of vector data
DATE-ISSUED: January 15, 1991

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FOREIGN-PRIORITY-APPL-DATE: July 29, 1987

INT-CL: [5] G06F012/00

US-CL-ISSUED: 364/200,364/231.9 ,364/232.21
US-CL-CURRENT: 712/6,712/200
FIELD-OF-SEARCH: 364/2MSFile;364/9MSFile

REF-CITED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4128880	December 1978	Gay, Jr.	364/200

14 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

BRIEF SUMMARY:
BACKGROUND OF THE INVENTION

The present invention is related to a computer for processing vector data.

In a conventional parallel computer sharing a main storage which is constituted by a plurality of vector processors, provision is made of a semaphore register that is shared by vector processors in the configuration. When a vector data written onto the main storage by a given vector processor in the configuration is to be read out by other vector processor, the semaphore register is used and the sequence of main storage references is ensured by effecting the exclusive control for the whole region where vector data of the main storage are stored. Apparatuses of this kind have been disclosed in U.S. Pat. No. 4,636,942 and S. Fernbach, "Supercomputers Class IV Systems, Hardware and Software", Elsevier Science Publishers B.V., Horth holland, 1986, pp. 69-81.

FIG. 5 illustrates how to use the abovementioned prior technology, wherein a VST instruction works to store the vector data in the main storage, a POST instruction works to finish the execution of the instruction after the main storage reference for all preceding instructions has been finished, a WAIT instruction works to finish the execution of the instruction after the execution of the POST instruction has been finished, and a VLD instruction works to load the vector data from the main storage. FIG. 5 is a time chart illustrating the operation in which two vector processors hand the vector data over via the main storage, and wherein an instruction sequence executed by a